

IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) A method, comprising:  
detecting at least one triggering signal by a multi-block memory comprising data, wherein said triggering signal comprises an event for multi-block memory activities but is not intended for memory wear leveling; and

copying or relocating, for said memory wear leveling, the data of at least one first memory block containing at least one memory element of the multi-block memory to at least one second memory block of the multi-block memory after detecting the at least one triggering signal every time said at least one triggering signal is detected, wherein said at least one second memory block does not contain said data before said copying or relocating,

wherein no information on a usage of said at least one first memory block, at least one second memory block or at least one memory element is provided for performing said copying or relocating.

2. (Previously Presented) The method according to claim 1, wherein each of the at least one first memory block and the at least one second memory block contains only one memory element.

3. (Previously Presented) The method according to claim 1, further comprising:

updating a first memory pointer M originally pointed to the at least one second memory block before said copying or relocating to point to the at least one first memory block after said copying or relocating.

4. (Previously Presented) The method according to claim 3, further comprising:

updating a second memory pointer Z by shifting it back to a physical zero point  $Z_0$  by reducing the value of the second memory pointer Z by a number of relocated memory elements of the second memory block if the first memory pointer M is pointing to one of the memory elements of the at least one second memory block after said updating.

5. (Previously Presented) The method according to claim 1, wherein there is more than one memory element contained in the at least one first memory block and there is more than one memory element contained in the at least one second memory block, respectively.

6. (Previously Presented) The method according to claim 1, wherein the data of an at least one additional block of the multi-block memory is relocated to an at least one further additional block of the multi-block memory after detecting the at least one triggering signal, wherein said at least one further additional block does not contain the data before said relocation.

7. (Previously Presented) The method according to claim 1, wherein said copying or relocating is performed according to a predetermined criterion.

8. (Previously Presented) The method according to claim 7, wherein said predetermined criterion enables said copying or relocating of a regular pattern such that after a predetermined number of triggering signals, said copying or relocating is identical to the copying or relocating performed in response to said predetermined number of the triggering signals.

9. (Previously Presented) The method according to claim 7, wherein said predetermined criterion enables said copying or relocating of a random pattern such that after any number of triggering signals, said copying or relocating is not identical to the copying or relocating performed in response to said any number of the triggering signals.

10. (Previously Presented) The method according to claim 1, wherein said copying or relocating of the data occurs only after detecting a predetermined number of the at least one triggering signal.

11. (Cancelled)

12. (Cancelled)

13. (Cancelled)

14. (Previously Presented) The method according to claim 1, wherein the at least one triggering signal is a

predetermined number of read/write operations or clock pulses.

15. (Previously Presented) The method according to claim 1, wherein said copying or relocating of the data occurs a predetermined number of times between triggering signals.

16. (Cancelled)

17 (Previously Presented) The method according to claim 1, wherein all the data contained in the multi-block memory is copied or relocated at the same time.

18. (Previously Presented) The method according to claim 1, further comprising:

updating a variable logical address X after said copying or relocating in the multi-block memory containing C memory elements, said variable logical address X for said C memory elements identified by pointers  $X_0, X_1 \dots X_k, X_{k+1} \dots X_{C-1}$  is updated to an updated variable logical address  $X_u$  for C-S memory elements identified by the pointers  $X_0, X_1 \dots X_{k-1}, X_{k+s} \dots X_{C-1}$ , wherein C is a total number of the memory elements of the multi-element memory, S is a number of the memory elements identified by the pointers  $X_k, X_{k+1}, \dots X_{k+s-1}$  in a spare memory block after said copying or relocating, wherein a first element of said first memory block after said copying or relocating corresponds to a first element identified by the pointer  $X_k$  of the spare memory spare block after said copying or relocating.

19. (Previously Presented) The method according to claim 1 wherein at least one memory pointer pointing to said first memory block before said copying or relocating is updated to point to said second memory block after said copying or relocating.

20. (Currently Amended) An electronic device, comprising:

a multi-block memory containing data, usable in multi-block memory activities;

a memory wear controller, responsive to a triggering signal or to a further triggering signal, wherein said triggering signal or said further triggering signal comprises an event for multi-block memory activities but is not intended for memory wear leveling, for providing a data-relocation signal to the multi-block memory for copying or relocating, for said memory wear leveling, the data from an at least one first memory block containing an at least one memory element of the multi-block memory to an at least one second memory block of the multi-block memory every time said triggering signal or said further triggering signal is detected, wherein said at least one second memory block does not contain said data before said copying or relocating, and for providing an update signal after performing said copying or relocating; and

a memory pointer controller, responsive to the update signal,

wherein no information on a usage of said at least one first memory block, at least one second memory block or at least one memory element is provided for performing said copying or relocating.

21. (Previously Presented) The electronic device of claim 20, wherein the memory pointer controller is configured to provide a pointer signal to the memory wear controller based on predetermined criteria.

22. (Previously Presented) The electronic device of claim 21, wherein the pointer signal comprises a physical address Y in the multi-block memory to be accessed for enabling an at least one further data relocation of the data located at the physical address Y and optionally further comprises an address of a first memory pointer M.

23. (Previously Presented) The electronic device of claim 20, wherein the memory pointer controller is configured to provide updating of at least one memory pointer pointing to said first memory block before said copying or relocating to point to said second memory block after said copying or relocating.

24. (Previously Presented) The electronic device of claim 20, wherein the memory wear controller and the memory pointer controller are implemented as a combination of software and hardware components.

25. (Previously Presented) The electronic device of claim 20, wherein the memory wear controller and the memory pointer controller are implemented as hardware.

26. (Previously Presented) The electronic device of claim 25, wherein the hardware is implemented using a finite state machine.

27. (Previously Presented) The electronic device of claim 20, wherein the memory wear controller and the memory pointer controller are implemented as software.

28. (Previously Presented) The electronic device according to claim 20, wherein each of the at least one first memory block and the at least one second memory block contains only one memory element.

29. (Previously Presented) The electronic device of claim 20, wherein there is more than one memory element contained in the at least one first memory block and there is more than one memory element contained in the at least one second memory block, respectively.

30. (Previously Presented) The electronic device of claim 20, wherein said copying or relocating of the data from the at least one first memory block and updating the location of the memory pointers M, Z are performed according to a predetermined criterion.

31. (Previously Presented) The electronic device of claim 20, further comprising a triggering detector, responsive to the triggering signal, for providing said further triggering signal upon detecting the triggering signal.

32. (Currently Amended) An electronic device, comprising:

means for containing data in multiple memory blocks, wherein said data is usable in activities of the means for containing data;

means for providing a data-relocation signal to the means for containing the data for copying or relocating, for memory wear leveling, the data from an at least one first memory block containing an at least one memory element of the means for containing the data to an at least one second memory block of the means for containing the data in response to a triggering signal or to a further triggering signal every time said triggering signal or said further triggering signal is detected, wherein said triggering signal or said further triggering signal comprises an event for multi-block memory activities but is not intended for said memory wear leveling, and wherein said at least one second memory block does not contain said data before said copying or relocating, and for providing an update signal on a status of the means for containing the data after performing said copying or relocating; and

means for controlling, responsive to the update signal, wherein no information on a usage of said at least one first memory block, at least one second memory block or at least one memory element is provided for performing said copying or relocating.

33. (Previously Presented) The electronic device according to claim 32, wherein the means for controlling further configured to provide updating of at least one memory pointer pointing to said first memory block before said copying or relocating to point to said second memory block after said copying or relocating.

34. (Cancelled)

35. (Cancelled)

36. (Previously Presented) The method of claim 1, wherein said event for said multi-block memory activities is at least one of: a) a write operation, b) a read operation; c) a clock pulse, d) a counter reaching a certain value and e) a counter counting read/write operations or clock pulses.

37. (Previously Presented) The electronic device of claim 20, wherein said event for said multi-block memory activities is at least one of: a) a write operation, b) a read operation; c) a clock pulse, d) a counter reaching a certain value and e) a counter counting read/write operations or clock pulses.